REMARKS

Status Summary

Claims 1-9 and 12-20 are pending in the present application, all of which presently stand rejected. Claims 1, 6, 7, and 20 are amended and new claim 21 is added by the present amendment. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the remarks set forth hereinbelow is respectfully requested.

Examiner Interview

Applicants appreciate Examiner He taking the time to discuss this application with their representatives, Jeff Wilson and Ben Aitken, during a telephone conference on August 25, 2009. During the interview, the parties discussed claims 1, 13, and 14 of the patent application and identified possible distinctions between the claimed subject matter and the subject matter of U.S. Patent Application Pub. No. 2005/10146346 to Kakizawa et at.. In particular, Applicants contended that the cited reference does not disclose switching transistors being switchable to provide a variety of different test signal paths for different test operation modes without requiring an external data loop back path.

Claim Rejections

Claims 1, 13, and 14 stand rejected by the Examiner under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Pub. No. 2005/10146346 to Kakizawa et at., hereinafter referred to as "Kakizawa". In addition, Claim 2 stands

rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Kakizawa in view of U.S. Patent No. 5,197,083 to Gandini et al., hereinafter referred to as "Gandini". Further, claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakizawa in view of applicants' admitted prior art hereinafter referred to as "AAP". These rejections are respectfully traversed.

Claim 1 has been amended to be reworded to more clearly recite that the plurality of switching transistors switch in a test mode an integrated termination resistor output stage to an integrated termination resistor input stage. Further, claim 1 has been amended to recite that the switching transistors are switchable and provide a plurality of different internal test signal paths within the test switching circuit between said input pad and said output pad corresponding to a plurality of test operation modes. Claim 13 has been corrected to recite that the reception data signal path is connected through an input pad. Also, claim 13 has been amended to recite that the plurality of switching transistors are switchable and provide a plurality of different internal test signal paths within the test switching circuit between said input pad and said output pad corresponding to a plurality of test operation modes. Finally, claim 14 has been similarly amended to recite that the plurality of switching transistors are switchable and provide a plurality of different internal test signal paths within the test switching circuit between said input pad and said output pad corresponding to a plurality of test operation modes. Support for these amendments can be found in the specification as originally filed, for example at page 21, line 34, though page 23, line 17, and in Figures 7-11.

As discussed in the interview, it is respectfully submitted that Kakizawa, taken either alone or in combination with one or both of Gandini or APA, fails to teach or suggest a plurality of switching transistors that are switchable and provide a plurality of *different* internal test signal paths *within the test switching circuit* between said input pad and said output pad corresponding *to a plurality of test operation modes*. It is respectfully requested that the rejection of claims 1, 13, and 14 under 35 U.S.C. § 102(b) should be withdrawn and the claims should be allowed at this time. Further, because claims 2-4 depend upon claim 1, it is respectfully requested that the rejection of claims 2-4 under 35 U.S.C. § 103(a) also be withdrawn and the claims allowed at this time.

Allowed Claims

Applicants again appreciate the Examiner's indication that claims 5-12 are allowable because none of the prior art discloses or fairly suggests a test switching circuit for a high speed data interface of an integrated circuit as is recited in these claims.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. 50-0426.

Respectfully submitted,

JENKINS, WILSON, TAYLOR & HUNT, P.A.

Date: 8-27-09 By: _____

Jeffrey L. Wilson
Registration No. 36,058
Customer No: 25297

1406/186 JLW/BJA/gwc